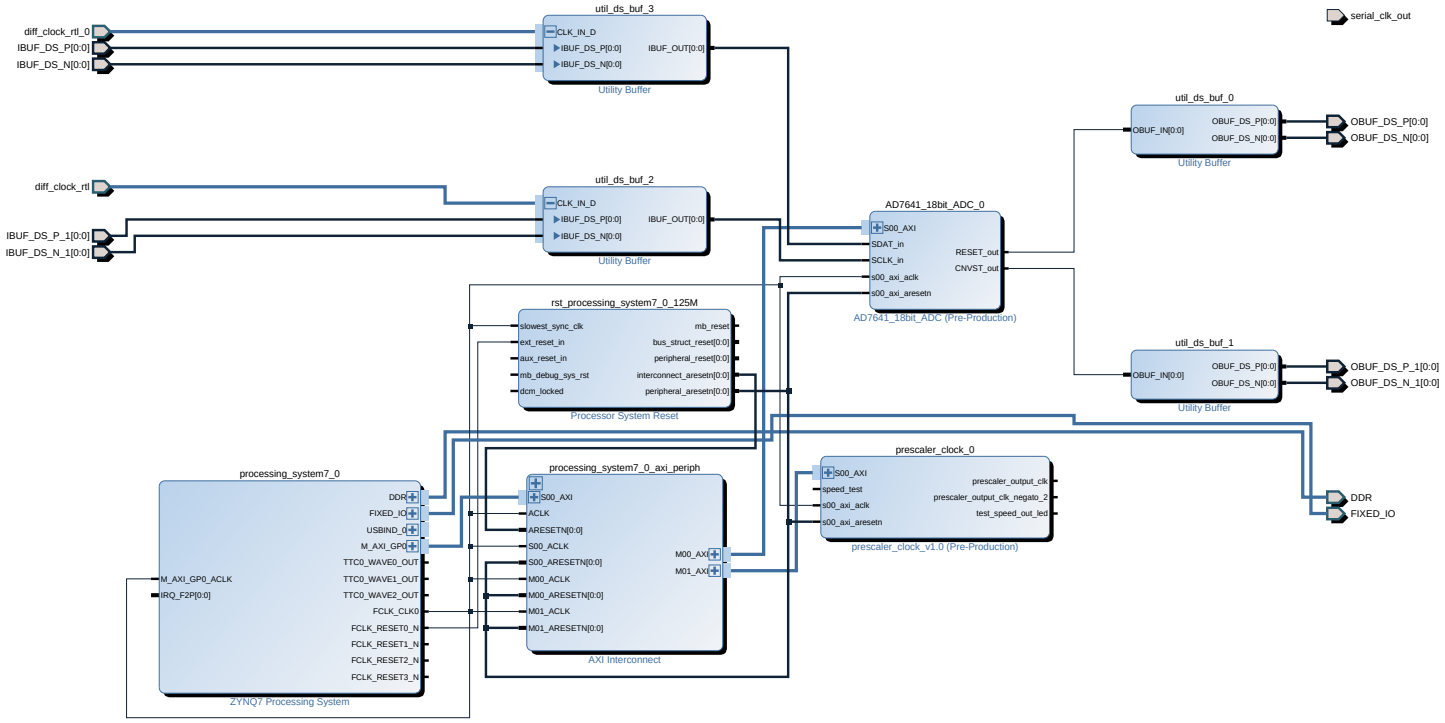
diff_clock_rtl_0
IBUF_DS_P[0:0]
IBUF_DS_N[0:0]
util_ds_buf_3
CLK_IN_D
IBUF_DS_P[0:0]
IBUF_DS_N[0:0]
IBUF_OUT[0:0]
Utility Buffer
serial_clk_out
util_ds_buf_0
OBUF_IN[0:0]
OBUF_DS_P[0:0]
OBUF_DS_N[0:0]
Utility Buffer
OBUF_DS_P[0:0]
OBUF_DS_N[0:0]
diff_clock_rtl
IBUF_DS_P_1[0:0]
IBUF_DS_N_1[0:0]
util_ds_buf_2
CLK_IN_D
IBUF_DS_P[0:0]
IBUF_DS_N[0:0]
IBUF_OUT[0:0]
Utility Buffer
AD7641_18bit_ADC_0
S00_AXI
SDAT_in
SCLK_in
s00_axi_aclk
s00_axi_aresetn
RESET_out
CNVST_out
AD7641_18bit_ADC (Pre-Production)
rst_processing_system7_0_125M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
util_ds_buf_1
OBUF_IN[0:0]
OBUF_DS_P[0:0]
OBUF_DS_N[0:0]
Utility Buffer
OBUF_DS_P_1[0:0]
OBUF_DS_N_1[0:0]
processing_system7_0
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
FCLK_RESET1_N
FCLK_RESET2_N
FCLK_RESET3_N
M_AXI_GP0_ACLK
IRQ_F2P[0:0]
ZYNQ7 Processing System
processing_system7_0_axi_periph
S00_AXI
ACLK
ARESETN[0:0]
S00_ACLK
S00_ARESETN[0:0]
M00_ACLK
M00_ARESETN[0:0]
M01_ACLK
M01_ARESETN[0:0]
M00_AXI
M01_AXI
AXI Interconnect
prescaler_clock_0
S00_AXI
speed_test
s00_axi_aclk
s00_axi_aresetn
prescaler_output_clk
prescaler_output_clk_negato_2
test_speed_out_led
prescaler_clock_v1.0 (Pre-Production)
DDR
FIXED_IO