**

Figure 4‑2 Analog frontend board block diagram.

*Observing the block diagram in above figure it is noted that the external connector has two pairs of signals in two pairs of input and output connections.*

*All of these pass through the LVDS driver in the pin indicated in the figure, on the isolated section of the field that is the one which will refer the masses and power supplies to the Zynq.*

|  |  |
| --- | --- |
| *LVDS output signals from* ***SN65LVDT*** | *Input control signals* ***SN65LVDT*** *(connector to Zynq)* |
| *SDATA +* | *CNVST+* |
| *SDATA -* | *CNVST-* |
| *SCLK +* | *RESET+* |
| *SCLK -* | *RESET-* |

Table 4‑1 Differential analog signals.

*RESET+ is connected to power down signal of the ADC, and the RESET- is connected, through flip-flop, on the SYN signal of the DC/DC converter, named DCV010505, useful for the isolation:*

*To filter signals (getting more square) and clean them from unexpected noise, it is necessary to going through the Flip/Flop before going to DCV01 that allow the connection towards other devices even off the board.*

*Setting the SYNCIN pin low the oscillator stops in order to turn off the card when not in use, it reacts in about 2 microseconds.*

*The other signals are passed in single ended and connected to the ADC through opto isolators.*

The ADC 7641 is the setting in pinMode [1: 0] = 11 so, from data book, (page 22), the system is placed in the operation mode ***MASTER SERIAL INTERFACE*** *- Internal Clock.*

*Other settings are Pin WARP = 1 and pin \_NORMAL = 0.*

*This configuration puts the chip at fasted speeds acquisition amounted to 2 MS/s, called WARP mode.*

*Insights are given on page 15 of the book, chapter MODES OF OPERATION.
Also from the schema:*

*\*EXT/INT =0 RDC/SDIN =1 INVSCLK = INVSYNC =0*

*\* To which reference is made to the timing shown in Xilinx Zynq databook, Fig. 36, p 23.*

## Interfacing the analog frontend to FPGA.

*To connect the analog on FPGA it must to generate on dedicated GPIO high signal to send to CNVST command pin. the ADC performs the conversion, and responds with a serial 18bit string of SDOUT-> SDATA, synchronized by the SCLK.*

*If you drive more frontend modules is need that the FPGA, for each one, produces a RESET output to enable the ADC, a CNVST output to start the conversion and two LVDS SDIN and SCLK inputs to connect to a 18 bit shift register to be defined in VHDL internally of the FPGA area.*

*The flow chart shows the signals and timings needed to obtain the 18bit string from the ADC*

## Frontend Low Pass Filter.



Figure 4‑3 Low pass filter schematic.

## Frontend to FPGA connector.



Figure 4‑6 Analog frontend to FPGA connector.

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Figure 4‑10 differential amp. op. schematic on insulated frontend.

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